Teresa M. Corbin (SBN 132360)
Christopher Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 147674)
Erik K. Moller (SBN 177927)
HOWREY SIMON ARNOLD & WHITE, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025
Telephone: (650) 463-8100
Facsimile: (650) 463-8400

Attorneys for Defendants AEROFLEX INCORPORATED, et al. and SYNOPSYS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

| | |
|---|---|
| RICOH COMPANY, LTD.,<br>Plaintiffs,<br><br>v.<br><br>AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTESM, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC.,<br>Defendants. | Case No. CV 03-04669 MJJ (EMC) |
| SYNOPSYS, INC.,<br>Plaintiff,<br><br>vs.<br><br>RICOH COMPANY, LTD.,<br>a Japanese corporation,<br>Defendant. | Case No. CV-03-02289 MJJ (EMC)<br><br>**DECLARATION AND SUMMARY OF OPINIONS OF DR. THADDEUS J. KOWALSKI ON CONSTRUCTION OF DISPUTED CLAIM TERMS OF UNITED STATES PATENT NO. 4,922,432** |

# DECLARATION AND SUMMARY OF OPINIONS OF DR. THADDEUS J. KOWALSKI ON CONSTRUCTION OF DISPUTED CLAIM TERMS OF UNITED STATES PATENT NO. 4,922,432

## I. INTRODUCTION AND EXPERT QUALIFICATIONS

1. My name is Thaddeus J. Kowalski, Ph.D. I have prepared this report in connection with my role as an expert witness on behalf of Synopsys, Inc. and Aeroflex, Inc., Aeroflex Colorado Springs, Inc., AMI Semiconductor Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. in Case Nos. C-03-2289-MJJ and C-03-4669-MJJ (collectively "Synopsys and Defendants") regarding United States Patent No. 4,922,432 ("the '432 patent"). I have summarized in this section my educational background, career history, publications, and other pertinent qualifications. A copy of my current resume is also attached as Attachment 1 to Exhibit A to the Joint Claim Construction and Prehearing Statement.[1]

2. I am the owner of Software Practices and Technology, LLC, a premier provider of technology evaluations, merger and acquisition evaluations, business turnarounds, business and technology strategy, and software and process development. Previously, I was the Vice President and Chief Technology Officer for Advanced Real-Time Communications Architecture and Strategy at AT&T Labs. I was responsible for incubation of new business services. While at AT&T, I led R&D efforts in support of numerous business and consumer initiatives.

3. I hold a master's degree in computer engineering as well as a doctorate in electrical engineering from Carnegie Mellon University. I authored a book on design automation, authored a book on rule-based programming, filed two dozen significant patents, published almost a hundred journal articles, and have given over two hundred technical presentations. As a researcher in Bell Telephone Laboratories I made significant contributions in the areas of artificial intelligence, operating systems, computer-aided design, programming and text-processing environments, speech processing, and real-time systems. I am also a member of the "Vulcans" engineering honor-service society, Eta Kappa Nu, and Phi Beta Kappa.

---

[1] Referenced attachments are attached to Exhibit A of the Joint Claim Construction and Prehearing Statement.

4. For more than 15 years, from about 1980 to 1996, I was involved in the field of computer-aided design of integrated circuits. During those years I spent significant time in both the commercial research and academic environments. While I worked at Bell Telephone Laboratories I was also a Ph.D. student at Carnegie-Mellon University. Bell Telephone Laboratories is known through out the world for its groundbreaking work in computer-aided and VLSI design. Carnegie-Mellon was one of the two best Universities in the country in artificial intelligence and computer-aided design. My thesis work involved using rule-based expert system techniques to create a seminal expert system that took an algorithmic description using hardware description languages (HDLs) and created VLSI chips. After completing my thesis, I broadened and extended that work for nearly 10 years at Bell Telephone Laboratories. My work was known worldwide and called the Design Automation Assistant. This worldwide reputation in computer-aided design and verification led to the supervision of six Ph.D. students in four countries. In addition to my thesis and about a hundred journal articles, I published ``An Artificial Intelligence Approach to VLSI Design,'' which was reprinted four times. I also coauthored a book on advanced rule-based programming techniques entitled ``Rule Based Programming.''

5. Through this experience, as detailed above and as set forth in my resume I have acquired expertise in the areas of the creation of computer-aided design tools to assist in the design of integrated circuits and rule-based expert systems.

## II. BACKGROUND TECHNOLOGY

6. I expect to provide background testimony regarding the state of the art of computer-aided design tools for designing integrated circuits using knowledge-based expert systems.

7. The processes of designing and manufacturing application specific integrate circuits (ASIC) are distinct processes that are both broad and complex. To make it easier to understand and give background, I will provide a description of the steps and processes to provide a helpful context. It is also my understanding from Synopsys' and Defendants' litigation counsel that Ricoh is claiming that the computer-aided design processes of the '432 patent are steps in manufacturing ASICs. In my expert opinion this is incorrect. Dr. Kobayashi, in a subsequent article, also has recognized that the

process of designing ASICs is separate from the processes for manufacturing an ASIC (CAD Tool Integration for ASIC Design: at 364-365 [Attachment 21]).

8. I will first explore the processes of designing ASICs and then briefly outline the processes of manufacturing ASICs. Designing ASICs can be described in two major steps, *i.e.*, specification capture followed by design synthesis and verification. Specification capture starts with a customer's need and a set of constraints. A designer will decide if the constraints will allow the customer's need to be realized as software on a general-purpose processor or as an application specific integrated circuit. If the constraints guide the designer to an ASIC design, a designer will typically codify the algorithm for the ASIC using some system to capture the operations and logical flows that show how to sequence the operations and specify them. The designer can also provide more detailed data that explicitly groups a sequence of operations to individual clock cycles. Next, the captured specification is synthesized and verified during design synthesis and verification. This step encompasses all the design phases, which successively map the captured specification into the photomask data. This step can be further subdivided into system, architecture, register transfer, logic, transistor, and layout levels. As the specification is mapped through these levels, technology, functional partitioning, module specification, and logic specification decisions are made. The logic is then placed and routed. The layout information is verified for consistency, correctness, and timing. The layout information is then rendered in a common physical design format so that the photomasks can be manufactured.

9. Before the manufacturing processes can begin a complex and costly process of creating photomasks is undertaken. This process transforms the physical design information into detailed instructions for the machine that creates the areas of light and dark on the photomasks. The photomasks are used over and over again in the manufacturing processes to create the transistor parts, circuit elements, insulating layers, and metallization paths necessary to fabricate the ASIC.

10. Manufacturing ASICs can be described in two major steps, *i.e.*, fabrication and the step of testing and verification. The fabrication process can be further subdivided into hundreds of phases. Highlights of these phases include: creating transistor parts, circuits elements, insulating layers, and

metallization paths by depositing layers of metal, oxide, and polysilicon on a substrate. Other highlights include thermal oxidation, lithography, etching, ion implantation, thermal redistribution, insulation, and metallization. The last step of the manufacturing processes tests and verifies the chip for environmental, stress, and defect problems.

## III. INFORMATION CONSIDERED IN FORMING OPINIONS

11. In forming the opinions set forth in this report, I have considered and reviewed the text of the '432 patent (attached to the Joint Claim Construction Statement as Attachment 2); the history of the prosecution of the application that led to the issuance of the '432 patent (attached to the Joint Claim Construction Statement as Attachment 3); and the prior art references that were before the patent office during the prosecution of the '432 patent (a few of which are attached to the Joint Claim Construction Statement as Attachments 4, 6-15, and 35. I also considered the related '016 patent (Attachment 5) and '669 patent (Attachment 23), which also relate to rule-based expert systems and lists Dr. Kobayashi (an inventor on the '432 patent) as an inventor. I also considered the November 1989 article authored by Dr. Kobayashi (Attachment 22), which in my expert opinion, describes the same basic KBSC system described in the '432 patent. Finally, I have also considered the dictionaries, technical dictionaries, technical treatises and textbooks, and technical articles identified in Synopsys' and Defendants' portion of the Joint Claim Construction Chart. The relevant portions of these are provided in Attachments 16-21 and 24-34.

## IV. OPINION AS TO LEVEL OF SKILL OF ONE OF ORDINARY SKILL IN THE ART

12. It is my understanding from Synopsys' and Defendants' litigation counsel that the proper construction of disputed claim terms requires determining the meaning of those disputed claim terms through the eyes of a person of ordinary skill in the art, *i.e.*, the pertinent scientific area, at the time the application for the '432 patent was filed, *i.e.*, January 1988. It is also my understanding from Synopsys' and Defendants' litigation counsel that the level of skill of a person of skill in the art may be determined based on one or more of the following factors: the educational level of the inventor; the type of problems encountered in the art; prior art solutions to those problems; the rapidity with which

innovations are made; sophistication of the technology; and the educational level of active workers in the field.

13. For purposes of interpreting the claims of the '432 patent, the pertinent scientific area is the creation of computer-aided design tools to assist in the design of integrated circuits. Typically, individuals of ordinary skill in this field would have a college degree (B.S. or M.S.) in a discipline such as Computer Science, Electrical Engineering, or Electrical and Computer Engineering and/or significant hands-on experience in creating large-scale software systems for assisting in the design of integrated circuits. In addition, individuals of ordinary skill in this field would have significant knowledge in programming, databases, user interfaces, and some knowledge of digital integrated circuit design.

## V. OPINIONS AS TO MEANING OF DISPUTED CLAIM TERMS IN THE '432 PATENT

14. It is also my understanding from Synopsys' and Defendants' litigation counsel that the claim terms should be construed in light of the intrinsic evidence of record, including the patent specification, drawings in the patent, the prosecution (or file) history, and prior art cited in the patent or file history. I have reviewed and relied upon materials listed in Section III. Using these resources, my knowledge of the field into which the patented invention falls and my own familiarity with the literature on computer-aided design tools to assist in the design of integrated circuits both prior to and after the filing date of the patent, and my familiarity with the level of ordinary skill in the art at the time the patent was filed, I have formed an opinion as to how one of ordinary skill in the art would have interpreted the claim terms at the time the application for the '432 patent was filed. My opinion as to each of the terms identified to me as being at least potentially in dispute by the parties to this case are provided in the following paragraphs.

15. The proper construction and support as to each of the terms identified to me as being at least potentially in dispute by the parties to this case are provided in Synopsys' and Defendants' portion of the Joint Claim Construction Chart. I arrived at these constructions through discussions between Synopsys' and Defendants' litigation counsel and myself. These constructions are also provided in the following paragraphs with some additional comments or discussion, where appropriate.

A. **"A computer-aided design process for designing"**

16. The meaning of this phrase is "a process that uses a computer for designing, as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process." This definition is not only supported by the definitions for computer-aided design (CAD) and computer-aided manufacturing (CAM) provided by Synopsys and Defendants, but is also supported by the dictionary definitions provided for those terms by Ricoh (IBM Dictionary at 129-130 [Attachment 16]; IEEE Dictionary at 180 [Attachment 19]). It is also consistent with the ordinary dictionary definitions for "designing" and "manufacturing" (Webster's Ninth New Collegiate Dictionary at 343, 725 [Attachment 20]).

17. Neither the '432 patent's specification nor its file history alters the ordinary meaning of this phrase. In fact, the '432 patent specification is consistent with and supports the ordinary meaning as set forth in the previous paragraph ('432 patent: 1:9-12 [Attachment 2]).

18. I disagree with the definition proposed by Ricoh for this phrase: "During the manufacture of a desired application specific integrated circuit (ASIC) chip that is designed to perform a specific purpose, a process of designing the desired ASIC using a computer." In particular, I disagree with Ricoh's attempt to equate or include computer-aided design processes for designing ASIC's with manufacturing ASICs. Designing an ASIC is a predicate process that creates the plan to make an ASIC. Specifically, the claimed processes of the '432 patent only produces the list of the necessary parts and their required interconnections and then uses that list to pictorially represent the physical placement of these necessary parts and the routing of their required interconnections. After additional complex processes, this information is eventually used to make the photomasks, or masks, that are used in the processes that manufacture the ASIC. The goal of the design process is to only have to make these masks once because of their cost, which for present day ASICs is about one million dollars. Manufacturing an ASIC entails the processes that physically implement the plan each time the ASIC is manufactured. Unlike the design processes, which are performed once, the processes that manufacture ASICs are repeated each time an ASIC is manufactured.

B. **"application specific integrated circuit"**

19. The meaning of this phrase is "an interconnected miniaturized electronic circuit on a single piece of semiconductor material designed to perform a specific function, as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc." The '432 patent specifically defines this phrase as "an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc." ('432 patent: 1:13-17 [Attachment 2]). Synopsys' and Defendants' definition for this phrase is the same but merely expands on this definition by providing a definition for "integrated circuit."

20. I disagree with Ricoh's definition, "an integrated circuit chip designed to perform a specific function," because it fails to explicitly exclude "general purpose integrated circuits, such as microprocessors, memory chips, etc." Ricoh's definition is contrary to the '432 patent, which provides the ordinary meaning for this phrase ('432 patent: 1:13-17 [Attachment 2]).

C. **"actions and conditions"**

21. "Actions and conditions" refer to "logical operations" or more specifically "logical steps and decisions." This is consistent with the definitions for "operations" provided by Synopsys and Defendants in their portion of the Joint Claim Construction Chart (IBM dictionary: at 479 [operations] [Attachment 16]). It is also consistent with the '432 patent's specification ('432 patent: 2:24-27; 4:15-19; 6:3-14; 8:47-51 [Attachment 2]). The limitation that these logical steps and decisions be "represented as rectangles and diamonds in the flowchart" is dictated by the '432 patent's file history. In particular, the '432 patent's file history unambiguously limits the input format to a flowchart format ('432 patent's file history: April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 [Attachment 3]). This is also consistent with the fact that the only adequately described input format in the '432 patent is the flowchart format ('432 patent: 3:50-59; 4:61-63; 7:20-23 [Attachment 2]). Although the '432 patent mentions a list type format ('432 patent: 2:21-24 [Attachment 2]) and appears to show a statelist in Appendix A ('432 patent: 14:7-30 [Attachment 2]), there is no description explaining that format in the '432 patent. In fact, such

explanation for the list format was only added in the later-filed, and related, '016 patent ('016 patent: 7:32-9:52 [Attachment 5]).

D. **"architecture independent"**

22. The phrase "architecture independent" was not in the originally filed application for the '432 patent. It was added to the application for the '432 patent in the abstract, the specification, and the claims as part of the April 1989 Amendment in the '432 patent's file history (April 1989 Amendment at pages 1-8 [Attachment 3]). This phrase is vague and imprecise and does not have a clear meaning. In addition, the '432 patent also does not provide a definition for this phrase.

23. "Architecture independent" is narrowly defined in the '432 patent's file history by the patent applicant's referencing and incorporating of the prior art '435 patent (Darringer et al.). Based on the file history and the '435 patent this phrase means: "not including (*i.e.*, excluding) a register transfer level (RTL) description or any other description that is hardware architecture dependent. An RTL description consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers; an RTL description defines any control needed for the ASIC" ('432 patent's file history: November 1989 Amendment at 7 [Attachment 3]). Specifically, the prior art '435 patent does describe an input specification that includes logical operations, *i.e.*, actions and conditions ('435 patent: Fig. 4; 4:26-32; 5:27-35 [Attachment 4]). The '432 patent claims were claimed by the patent applicant to be different from the '435 patent because, among other things, the phrase "architecture independent" was added to the claims. The patent applicant also stated that the prior art '435 patent's input specification included a register-transfer level description and therefore, that the '435 input specification was hardware architecture dependent, in contrast to the patent applicant's architecture independent specification (April 1989 Amendment at 8-10, 13; November 1989 Amendment at 7 [Attachment 3]).

24. In other words, the input specification of the prior art '435 patent was claimed to be different from the input specification of the '432 patent because, unlike the prior art '435 patent, the

input specification of the '432 patent only consists of logical operations and excludes a register-transfer level description.

25. I disagree with Ricoh's proposed definition for "architecture independent actions and conditions" and Ricoh's incorporation of that definition into the definition of the phrase "a set of definitions of architecture independent actions and conditions." Ricoh's definition provides: "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure, or implementing technology." First, Ricoh's proposed definition fails to acknowledge the limitations from patent applicants statements in the '432 patent's file history. As discussed in Paragraphs 21 and 23, these statements limit the input specification and therefore, the "actions and conditions" to a flowchart format. Second, Ricoh's proposed definition fails to recognize that "architecture independent" was narrowly defined in the '432 patent's file history as excluding a register-transfer level description as defined in the prior art '435 patent. Without the file history statement, the phrase "architecture independent" is vague and imprecise and is not defined in the '432 patent. Third, Ricoh appears to equate "architecture independent" with the equally imprecise and vague phrase "does not imply any set architecture, structure, or implementing technology" and which is also contrary to the definition claimed in the '432 patent's file history and not supported by any description in the '432 patent's specification. Finally, Ricoh's definition uses the vague and imprecise phrase "functional or behavioral aspects of a portion of a circuit," which is neither consistent with nor supported by the description in the '432 patent (2:24-27; 4:15-19; 6:3-14; 8:47-51 [Attachment 2]).

26. I also do not agree with Ricoh's definition for the word "storing" in a number of the claim steps: "placing in computer memory." In particular, "storing" means "placing data in any storage device" that is accessible by the processor in the computer system (IBM Dictionary of Computing at 654 [Attachment 16]).

E. **"a set of definitions of architecture independent actions and conditions"**

27. This entire phrase, incorporating the above definitions, means: "a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart; and excluding a register transfer level description." This is

consistent with the '432 patent's specification ('432 patent: 4:61-63; 5:20-22; 6:3-14; 7:25-50; 8:47-51[Attachment 2]).

28. I disagree with Ricoh's definition for this entire claim step. That disagreement stems from Ricoh's incorporations of its definitions for "storing" and "architecture independent actions and conditions" as discussed in Paragraphs 25-26.

F. **"hardware cells"**

29. "Hardware cells" refers to the "logic blocks for which the functional level (e.g., register transfer level), logic level (e.g., flip flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) descriptions are all defined." This definition is consistent with the '432 patent's requirement that "previously designed, tested, and proven hardware cells" are defined in the cell library ('432 patent: 5:15-20 [Attachment 2]). The '432 specification and the other steps in claims 13-17 also require that the hardware cells must be defined with the following types of information: functional level, logic level, circuit level, and layout level ('432 patent: 2:34-39; 3:59-67; 9:24-51; 16:60-68 [Attachment 2]).

30. My disagreement with Ricoh's definition for this term, "previously designed circuit components or structure that have specific physical and functional characteristics used as building blocks for implementing an ASIC to be manufactured" includes the use of the phrase "specific physical and functional characteristics." The '432 patent's described method for designing an application integrated circuit requires the hardware cells in the cell library to be previously designed, tested, and proven logic blocks ('432 patent: 5:15-20 [Attachment 2]). This means that those hardware cells must be defined with the following types of information: functional level, logic level, circuit level, and layout level ('432 patent: 2:34-39; 3:59-67; 9:24-51; 16:60-68 [Attachment 2]). I also disagree with the use of the phrase "for implementing an ASIC to be manufactured." As explained in Paragraphs 16-18, the '432 patent claims 13-17 encompass computer-aided design processes for designing an ASIC and not manufacturing them.

G. **"data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set"**

31. This claim phrase means "a set of named integrated circuit hardware cells that includes at least one hardware cell for each stored definition that may be specified for the available logical steps and decisions; where each named hardware cell has corresponding descriptions at the functional level (e.g., register transfer level), logic level (e.g., flip-flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) that are all defined." The '432 patent specification requires that there be one or more defined hardware cells corresponding to each of the stored definitions that may be specified ('432 patent: Fig. 4; 5:23-25 [Attachment 2]). The '432 specification and the other steps in claims 13-17 also require that the data describing the hardware cells must define the following types of information: functional level, logic level, circuit level, and layout level ('432 patent: 2:34-39; 3:59-67; 9:24-51; 16:60-68 [Attachment 2]).

32. I disagree with Ricoh's proposed definition, "a library of cell information that describe hardware cells capable of performing the different architecture independent actions and conditions placed in the library of definitions," because Ricoh fails to include a requirement that there is at least one corresponding hardware cell description for each of the stored definitions that may be specified. Similar to its definition for hardware cell, Ricoh's definition again fails to specify what constitutes the "data describing" the available hardware cells as I explained in Paragraph 33.

H. **"expert system"**

33. The meaning of an expert system is: "software executing on a computer system that attempts to embody the knowledge of a human expert in a particular field and then uses that knowledge to simulate the reasoning of such an expert to solve problems in that field. This system is comprised of a knowledge base containing rules, working memory containing the problem description, and an inference engine. It solves problems through the selective application of the rules in the knowledge base to the problem description, as distinguished from conventional software, which uses a predefined step-by-step procedure (algorithm) to solve problems." This ordinary meaning is apparent from the texts, dictionaries, and articles from that time period as well as the Dr. Kobayashi's own

article from the same time his application for the '432 patent was pending (Computer Aided VLSI Design Vol.1 No. 4: 351, 377-381, 383, 388-389 [Attachment 22]; '669 patent: Abstract, 1:13-16, 2:28-33, 4:31-62; 5:21-38, 5:58-68, 6:1-7:68, 17:62 [Attachment 23]; Understanding Expert Systems: 7-10, 29-30, 40, 42, 74-78, 99-110 [Attachment 24]; An Artificial Intelligence Approach To VLSI Design: at 9-15 [Attachment 25]; Artificial Intelligence Terminology: at 6 [algorithm], 10 [antecedent], 53 [consequent], 86-87 [expert system], 127 [inference engine], 140 [knowledge based system], 204 [production system], 223 [rule base, rule-based system], 281 [working memory] [Attachment 26]; Microsoft Press Computer Dictionary: at 136 [expert system] [Attachment 27]; IBM Dictionary of Computing: 591 [rule interpreter, rule-based system] [Attachment 16]; The VLSI Design Automation Assistant: at 34 [Attachment 28]; A Rule-Based Logic Circuit Synthesis System for CMOS Gate Arrays: at 597 [Attachment 29]; Expert Systems: A Non-Programmer's Guide: 8-10, 16 [Attachment 30]; Expert Systems: Tools and Applications: at 269 [Attachment 31]; Expert Systems: Principles and Case Studies: at 11-12 [Attachment 32]; Knowledge-Based Systems: The View in 1986: at 16 [Attachment 33]). In particular, Mr. Kobayashi's article states that there are only "two different types of approaches to automatic logic synthesis: algorithmic and rule-based. IF-THEN-type rules rather than algorithmic programming languages are used in the latter approach to synthesize logic circuits" (Computer Aided VLSI Design Vol.1 No. 4: at 351 [Attachment 22]). Mr. Kobayashi also states that the KBSC method described in this article and in his patent "is clearly distinguished from other logic synthesis systems in terms of its flowchart input form and rule-based approach to automatic data-path and control logic synthesis" (Computer Aided VLSI Design Vol.1 No. 4: at 389 [Attachment 22]).

34. The '432 patent's specification and the claims also support this ordinary meaning for the term expert system ('432 patent: 2:58-63; 5:6-8; 8:58-60; 10:39-11:26; 14:50-59; 15:53-58[Attachment 2]).

35. The '432 patent's file history and the prior art references referred to in that file history also dictate this definition for the term "expert system" (April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3]; '435 patent: 7:32-9:35 [Attachment 4]; An Overview of Logic Synthesis Systems: at 170 [Attachment

7]; The CMU Design Automation System: at 75-77 [Attachment 8]). In particular, the patent applicant states numerous times and the patent examiner agreed in the '432 patent's file history that a rule-based expert system was required for translating the flowchart into a netlist. I would also like to point out that in the 1988 time frame the terms "expert system," "rule-based expert system," "knowledge based expert system," and "production system" were all used interchangeably to refer to an "expert system" as defined in Paragraph 33.

I. **"knowledge base"**

36. The meaning of the term "knowledge base" is "the portion of the expert system containing a set of rules embodying the expert knowledge for the particular field." This ordinary meaning is apparent from the texts from the 1988 time period as well as Dr. Kobayashi's own related '669 patent, which was filed about the same time as his application for '432 patent was filed ('669 patent: Abstract [Attachment 23]).

37. The '432 patent's specification and the claims also support this ordinary meaning for the term knowledge base ('432 patent: 10:39-11:15 [Attachment 2]).

38. The '432 patent's file history and the prior art references referred to in that file history also dictate this definition for the term "knowledge base" ('432 patent's file history: April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3]; '435 patent: 7:32-9:35 [Attachment 4]).

39. I disagree with Ricoh's definition for the term "expert system knowledge base," which provides: "database used to store expert knowledge of highly skilled VLSI designers." First, Ricoh's definition fails to acknowledge that a knowledge base is just one portion of the rule-based expert system; specifically, the portion containing the IF-THEN rules embodying the expert knowledge ('432 patent: 14:50-59; 15:53-58 [Attachment 2]). The file history requires that a rule-based expert system be used (April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3]). Second, Ricoh's definition fails to include a definition for "expert system" and all of the necessary portions required for such a system based upon the ordinary meaning of "expert system" set forth in Paragraph 33. Third, Ricoh's definition is

inaccurate because it fails to require that the knowledge base store the expert knowledge in the form of IF-THEN rules. This is contrary to the '432 patent specification, the other claims, the '432 patent's file history, and the inventors own article and his related patent from that period (Computer Aided VLSI Design Vol.1 No. 4: 351, 377-381, 383, 388-389 [Attachment 22]; '669 patent: Abstract, 1:13-16, 2:28-33, 4:31-62; 5:21-38, 5:58-68, 6:1-7:68, 17:62 [Attachment 23]).

40. Ricoh's definition also contradicts the patent applicant's own claims that the prior art '435 patent (Darringer et al.) differed because it did not provide a "knowledge base of any kind" or a "rule-based expert system" ('432 patent's file history: April 1989 Amendment at 9-10 [Attachment 3]). The prior art '435 patent contained "expert knowledge of highly skilled VLSI designers," which is referred to as transforms ('435 patent: 7:32-9:35 [Attachment 4]). Ricoh's definition is too broad because it would encompass the "transforms" described in the prior art '435 patent, which the patent applicant claimed were not a knowledge base.

J. **"a set of rules for selecting hardware cells to perform the actions and conditions"**

41. The meaning of this phrase is: "a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description." This definition is consistent with the ordinary meaning of the term "rules" when referring to the rules that are contained in the knowledge base of a rule-based expert system (Expert Systems: A Non-Programmer's Guide: 8-10, 16 [Attachment 30]; Expert Systems: Principles and Case Studies: at 11-12 [Attachment 32]). The definition is also consistent with the inventor's article published while the '432 patent application was pending (Computer Aided VLSI Design Vol.1 No. 4: 351, 377-381, 383, 388-389 [Attachment 22]). In particular, the quote from Paragraph 33 of the Dr. Kobayashi's article shows that the KBSC method described there and in the '432 patent was limited to using IF-THEN type rule to codify the expert knowledge of ASIC designers.

42. The definition of this phrase is also consistent with the '432 patent's specification and required by the other claimed steps and other claims ('432 patent: 2:58-63; 8:20-30; 8:58-9:62; 10:39-11:26; 14:50-59; 15:53-58; 16:34-65 [Attachment 2]).

43. The '432 patent's file history and the prior art references, in that file history, also dictate the definition for this phrase ('432 patent's file history: April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3]; '435 patent: 7:32-9:35 [Attachment 4]; An Overview of Logic Synthesis Systems: at 170 [Attachment 7]; The CMU Design Automation System: at 75-77 [Attachment 8]).

44. I disagree with Ricoh's definition for this phrase: "a plurality of rules for selecting among the hardware cells placed in the hardware cell library, wherein the rules comprise the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures." First, Ricoh's definition of "rule" is contrary to the ordinary meaning for that term when applied to rule-based expert systems (Expert Systems: A Non-Programmer's Guide: 8-10, 16 [Attachment 30]; Expert Systems: Principles and Case Studies: at 11-12 [Attachment 32]). Second, Ricoh's definition for "rule" is also inconsistent with the '432 patent's file history. Specifically, Ricoh's definition for "rule" provides: "the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures." This contradicts patent applicant's claims that the prior art '435 patent (Darringer et al.) differed because it did not provide a "knowledge base of any kind" or a "rule-based expert system" ('432 patent's file history: April 1989 Amendment at 9-10 [Attachment 3]). The prior art '435 patent does contain "expert knowledge of highly skilled VLSI designers formulated as prescribed procedures" ('435 patent: 7:32-9:35 [Attachment 4]). The '435 patent refers to the expert knowledge of highly skilled VLSI designers as "transforms" and the prescribed procedures as "scenarios." Ricoh's definition is too broad because it would encompass the "transforms" and "scenarios" described in the prior art '435 patent, which the patent applicant claimed were not a knowledge base.

45. I also disagree with Ricoh's definition for this phrase because Ricoh does not require that the set of "rules" be for mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description. This is inconsistent

with the '432 patent specification, claim 13, and the other claims ('432 patent: 2:58-63; 8:20-30; 8:58-9:62; 10:39-11:26; 14:50-59; 15:53-58; 16:34-65 [Attachment 2]).

K. **"describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions"**

46. The meaning of this phrase is: "the designer represents a sequence of logical steps (rectangles) and decisions (diamonds), and the transitions (lines with arrows) between them in a flowchart format for a proposed application specific integrated circuit." This definition is consistent with the '432 patent's only adequately described input specification. This definition is dictated by the claim language in claim 13 and the patent applicant's statements in the '432 patent's file history ('432 patent: Figs. 1a, 5, &7; 2:21-27; 3:20-22; 3:50-59; 4:5-22; 4:35-38; 7:12-23; 16:34-65 [Attachment 2]; '432 patent's file history: April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 [Attachment 3]).

47. This definition is also consistent with the dictionary definitions of the words "series," "sequence," and "describing" (Webster's Ninth New Collegiate Dictionary at 1074, 1073, 343 [Attachment 20]).

48. I disagree with Ricoh's definition for this claim step, which provides: "a user describing an input specification containing the desired functions to be performed by the designed ASIC." First, Ricoh's definition incorrectly provides that the "desired functions to be performed" are contained in this step. This is contrary to the '432 patent's specification and the claim language. Second, Ricoh's definition ignores the words "series" and "conditions" and fails to acknowledge that this step is for describing, or representing, the sequence of logical steps and decisions and the transitions between them. This definition is also contrary to the '432 patent's specification and the claim language. Third, Ricoh's definition does not provide for the limitation required by the '432 patent's file history that the sequence of logical steps and decisions and the transitions between them must be represented or described in a flowchart format ('432 patent's file history: April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 [Attachment 3]).

49. Ricoh's definition is also incorrect because it leaves out critical information. Specifically, describing the sequence of the steps and decisions is necessary for producing the control signals required for the ASIC. This sequence information for the steps and decisions is critical because these steps and decisions are required to be "architecture independent," excluding a register-transfer level description.

L. **"specifying for each described action and condition of the series one of said stored definitions"**

50. The meaning of this phrase is: "the designer assigns one definition from the set of stored definitions for each of the described logical steps and decisions represented in the flowchart." This definition is consistent with the '432 patent's only adequately described input format and dictated by the claim language in claim 13 ('432 patent: Fig. 5; 3:20-22; 4:61-63; 5:20-22; 7:24-25; 8:23-26; 8:51-56 [Attachment 2]).

51. I disagree with Ricoh's definition for this claim step: "specifying for each desired function to be performed by the desired ASIC one of the definitions of the architecture independent actions and conditions stored in the library of definitions that is associated with the desired function." First, Ricoh's definition reiterates the same inaccuracies from the previous describing step. Second, Ricoh's definition contradicts the '432 patent's specification by failing to acknowledge that the designer separately assigns the stored definitions to each logical step and decision. In addition, the claim language clearly provides that this assigning step must occur after the series of logical steps and decisions have been described (or represented).

52. I also disagree with Ricoh's definition for "specifying": "mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions." The claim language and the '432 patent specification make clear that this step is performed by the user assigning the stored definitions to each of the described logical steps and decisions ('432 patent: Fig. 5; 3:20-22; 4:61-63; 5:20-22; 7:24-25; 8:23-26; 8:51-56 [Attachment 2]). This "specifying" step is part of input specification provided by the user for the desired ASIC to be designed and cannot be performed by the system described in the '432 patent. Ricoh's definition is

also contrary to the dictionary definitions of "specify" and "specification" Webster's Ninth New Collegiate Dictionary at 1132 [Attachment 20]). Finally, I also disagree with Ricoh's adding of the phrase "performed by a manufactured ASIC." As explained in Paragraphs 16-18, the '432 patent claims 13-17 encompass computer-aided design processes for designing an ASIC and not manufacturing them.

M. **"which corresponds to the desired action or condition to be performed"**

53. The meaning of this phrase is: "each specified definition must correspond to the intended step or decision to be performed." This definition is consistent with the ordinary meaning of the terms, the '432 patent specification, and required by the language of the claims ('432 patent: Fig. 5; 3:20-22; 4:61-63; 5:20-22; 7:24-25; 8:23-26; 8:51-56; 16:34-65 [Attachment 2]).

54. Ricoh's definition, which is provided in Paragraph 51, is incorrect because it replaces "correspond to" with the phrase "associated with." The claim language and the '432 patent specification and the ordinary meaning of these terms all require that the definitions assigned must correspond to (or match) what is intended for each logical step or decision (Webster's Ninth New Collegiate Dictionary at 110 [associate], 293 [correspond] [Attachment 20]).

N. **"selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit"**

55. The meaning of this phrase is: "mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description." This definition is consistent with the '432 patent's only adequately described system and dictated by the claim language in claim 13 ('432 patent: Fig. 4; 3:16-19; 4:66-5:3; 5:22-29; 8:31-37; 8:58-60; 9:52-60; 16:34-65 [Attachment 2]) '432 patent file history: April 1989 Amendment at 10 [Attachment 3].

O. **"said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base"**

56. The meaning of this phrase is: "the mapping of the specified definitions to the stored hardware cell descriptions must be performed by an expert system having an inference engine for selectively applying a set of rules, each rule having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description." This definition is consistent with the '432 patent's only adequately described system and dictated by the claim language in claim 13 and the patent applicant's statements in the '432 patent's file history ('432 patent: Abstract; 2:58-63; 5:6-8; 8:29-37; 8:58-60; 9:8-13; 11:16-26; 16:34-65 [Attachment 2]; '432 patent's file history: April 1989 Amendment at 8-11, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 4, 6-7, 9 [Attachment 3]; '435 patent: 7:32-9:35 [Attachment 4]).

57. Ricoh's combined definition for both N and O provides: "selecting from the plurality of hardware cells in the hardware cell library a hardware cell for performing the desired function of the desired ASIC through the application of the rules." This definition is not correct and leaves out numerous requirements. First, Ricoh's definition fails to require that the mapping be performed for "each specified definition." This is required by both the claim language itself and the '432 patent specification. Second, Ricoh's definition also fails to limit how the "mapping" is performed. Specifically, that the mapping must be accomplished using a rule-based expert system ("432 patent's file history: April Amendment at 10 [Attachment 3]). Third, Ricoh's definition is contrary to the ordinary meaning of "expert system" and the statements in the '432 patent's file history because it fails to require that the applying of the "set of cell selection rules" in the knowledge base of the rule-based expert system is performed by that rule-based expert system's inference engine (Paragraphs 33-35).

P. **"netlist"**

58. The meaning of this phrase is: "a structural description that includes a custom controller type hardware cell and all other hardware cells required to implement the application specific integrated circuit's operations and any necessary interconnections including the necessary control and data path information for connecting the hardware cells and the controller." This definition is consistent with the '432 patent's only adequately described system as well as the claims ('432 patent: Abstract; 1:17-37; 2:39-44; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 12:31-35; 13:55-14:3; 16:34-65 [Attachment 2]).

59. Ricoh's definition, which is: "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc." is not correct. First, Ricoh's definition fails to require that there is a description for the controller type hardware cell, which is needed to provide the control for the other needed hardware cells as required by the '432 patent specification. Second, the '432 patent also clearly requires that the netlist must provide the structural description of the control paths and data paths that connect the controller type hardware cell and the other needed hardware cells.

60. I also disagree with the use of the phrase "needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc." As explained in Paragraphs 16-18, the '432 patent claims 13-17 encompass computer-aided design processes for designing an ASIC and not manufacturing them.

Q. **"generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit"**

61. The meaning of this phrase is: "producing a list of the needed hardware cells by eliminating any mapped hardware cells that are redundant or otherwise unnecessary and producing a custom controller type hardware cell for providing the needed control for those other hardware cells." This definition is consistent with the '432 patent's only adequately described system and dictated by

the claim language in claim 13 ('432 patent: Abstract; 1:17-37; 2:39-44; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 13:55-14:3; 16:34-65 [Attachment 2]).

62. Ricoh's definition, which is: "generating a netlist that identifies the hardware cells needed to perform the function of the desired ASIC and the necessary parameters for connecting the respective inputs and outputs of each hardware cell, the netlist is passed to the next subsequent step in the process for manufacturing the desired ASIC" is not correct. First, contrary to the claim language, "for the selected cells," Ricoh's definition fails to require that generation step must follow the prior step of selecting (mapping) the hardware cell descriptions and therefore, performed using those selected (mapped) hardware cell descriptions. Instead, Ricoh's definition, contrary to the claim language and the '432 patent's specification, provides that the generation step is performed without any connection to this prior step. Second, Ricoh's definition does not require that the controller type hardware cell be generated. This is also contrary to the requirements in the '432 patent's specification and the definition of "netlist" as required by the '432 patent's specification. Third, again contrary to the '432 patent's specification and the claim language, Ricoh's definition fails to require that the "hardware cells which are needed" are the selected (mapped) hardware cell descriptions that remain after any unnecessary or redundant hardware cell descriptions have been eliminated.

R. **"generating...interconnection requirements therefor"**

63. The meaning of this phrase is: "producing the necessary structural control paths and data paths for the needed hardware cells and the custom controller." This definition is consistent with and required by the claim language and the '432 patent's specification ('432 patent: Abstract; Figs. 6 & 13-15; 1:17-37; 2:39-44; 3:23-25; 3:40-45; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 13:55-14:3; 16:34-65 [Attachment 2]).

64. I do not agree with the Ricoh's definition and specifically the part that provides: "the necessary parameters for connecting the respective inputs and outputs of each hardware cell." The "interconnection requirements" for the needed hardware cells netlist must include the structural control paths and data paths connecting those cells. Otherwise, it would not be a netlist as defined in Paragraph 58.

S. **"generating from the netlist the mask data required to produce an integrated circuit having the desired function"**

65. The meaning of this phrase is: "producing, from the structural netlist, the detailed layout level geometrical information required for manufacturing the set of photomasks that are used by the processes that directly manufacture the application specific integrated circuit." This definition is consistent with the ordinary meaning of the phrase "mask data" and is also consistent with the minimal information provided by the '432 patent specification on what is meant by "mask data" ('432 patent: Abstract; Fig. 1c; 1:42-44; 1:54-58; 2:44-49; 4:44-46; 5:40-46; 14:4-6; 16:34-68 [Attachment 2]).

66. Ricoh's definition, which is: "producing from the netlist of hardware cells to be included in the designed ASIC mask data which can be directly used by a chip foundry in the fabrication of the ASIC" is not correct. First, Ricoh's definition does not define "mask data." Second, "mask data" is only the information or data that can be used by other complex processes for making photomasks for the designed application specific integrated circuit. Mask data cannot be used to fabricate or manufacture an application specific integrated circuit.

T. **"generating data paths for the selected integrated circuit hardware cells"**

67. The meaning of this phrase is: "producing the necessary structural descriptions of the data paths for the selected hardware cells." This definition is consistent with the ordinary meaning and is also consistent with the '432 patent specification ("432 patent: Abstract; 2:39-40; 4:63-66; 5:6-12; 5:30-37; 6:29-31; 6:37-43; 6:50-53; 9:62-10:9; 13:55-14:3; 16:34-17:3 [Attachment 2]).

68. Ricoh's definition, which is: "producing signal lines for carrying data to the hardware cells" is not correct. First, Ricoh's definition ignores the claim language "for the selected integrated circuit hardware cells." Second, the processes of the '432 patent are for producing design data and not the physical "signal lines for carrying data" (IEEE Standard Dictionary at 898 [signal line] [Attachment 19]). As explained in Paragraphs 16-18, the '432 patent claims 13-17 encompass computer-aided design processes for designing an ASIC and not manufacturing them.

U. **"said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom"**

69. The meaning of this phrase is: "the generating step must be performed by at least an expert system having an inference engine for selectively applying a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to produce the necessary data paths for the mapped hardware cells." This definition is consistent with the '432 patent's only adequately described system and dictated by the claim language in this claim and the patent applicant's statements in the '432 patent's file history ('432 patent: Abstract; 5:6-12; 9:62-10:9; 13:55-14:3 [Attachment 2]; '432 patent's file history: April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3]; '435 patent: 7:32-9:35 [Attachment 4]; An Overview of Logic Synthesis Systems: at 170 [Attachment 7]; The CMU Design Automation System: at 75-77 [Attachment 8]).

70. Ricoh's definition provides: "wherein the step of producing signal lines for carrying data comprises applying rules, which are placed in computer memory, to produce the signal lines for carrying data to the hardware cells." This definition is not correct and leaves out numerous requirements. First, Ricoh's definition incorporates the same incorrect statements about the "data paths" from the definition of claim 15, which I explained in Paragraph 68. Second, Ricoh's definition also fails to limit how the "mapping" is performed. Specifically, that the mapping must be accomplished using a rule-based expert system ('432 patent's file history: April Amendment at 10 [Attachment 3]). Third, Ricoh's definition is contrary to the ordinary meaning of "expert system" and the statements in the '432 patent's file history because it fails to require that the applying of the "set of data path rules" in the knowledge base of the rule-based expert system is performed by that rule-based expert system's inference engine. Fourth, Ricoh's definition fails to require that the "rules" are stored in the knowledge base of the rule-based expert system.

V. **"generating control paths for the selected integrated circuit hardware cells"**

71. The meaning of this phrase is: "producing the necessary structural descriptions of the control paths for the selected hardware cells." This definition is consistent with the ordinary meaning and is also consistent with the '432 patent specification ('432 patent: Abstract; Figs. 1b & 13-15; 1:17-37; 2:40-42; 3:59-65; 4:39-43; 4:63-65; 5:3-12; 5:30-36; 6:18-27; 11:49-51; 13:51-14:3 [Attachment 2]).

72. Ricoh's definition: "producing signal lines for carrying control signals to the hardware cells" is not correct. First, Ricoh's definition ignores the claim language "for the selected integrated circuit hardware cells." Second, the processes of the '432 patent are for producing design data and not physical "signal lines for carrying control signals." As explained in Paragraphs 16-18, the '432 patent claims 13-17 encompass computer-aided design processes for designing an ASIC and not manufacturing them.

73. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on July 13, 2004, at Summit, New Jersey.

/s/ Thaddeus J. Kowalski
Thaddeus J. Kowalski